CLAIMS

1. A bus system that transfers data between a plurality of semiconductor devices, wherein:

a first wiring is drawn out of a first semiconductor, a plurality of wirings are arranged in parallel with the first wiring to constitute directional couplers, and the wirings are each connected to a second semiconductor device; and

each of the directional couplers has a different coupling length so that signal amplitudes generated by the plurality of directional couplers may be substantially the same.

2. The bus system according to claim 1, wherein when it is assumed that lengths of n directional couplers connected are L1, L2, L3, … Ln in the order nearer to the first semiconductor, generated signal amounts of the directional couplers are substantially the same by satisfying $L1 \leqq L2 \leqq L3 \leqq \ldots \leqq Ln$.

3. The bus system according to claim 2, wherein when it is assumed that the second semiconductor comprises four second semiconductors, and lengths of the directional couplers are L1, L2, L3 and L4 in the order nearer to the first semiconductor, a difference among the coupling lengths of L1, L2, L3 and L4 is within 10 mm.

4. The bus system according to claim 1, wherein when it is assumed that intervals between two parallel lines that constitute n directional couplers connected are w1, w2, w3, … wn in the order nearer to the first semiconductor, the degrees of coupling of the directional couplers are changed by satisfying $w1 \geqq w2 \geqq w3 \geqq \ldots \geqq wn$, and generated signal amounts of the directional couplers are substantially the same.

5. The bus system according to claim 4, wherein when it is assumed that the degree of coupling of an i-th directional coupler from the first semiconductor is Kbi, the i-th directional coupler has the degree of coupling Kbi given by $Kbi = Kbi * (1 + (i - 1) * x)$, where the degree of coupling Kb1 of the first directional coupler has a coefficient of $x = 0.1$ to 0.2.

6. A printed circuit board in the bus system of claim 2 or 3, wherein the directional couplers have the coupling lengths that satisfy $L1 \leqq L2 \leqq L3 \leqq \ldots \leqq Ln$.

7. A printed circuit board in the bus system of claim 4 or 5, wherein the directional couplers are provided which have the wiring intervals that satisfy $w1 \geqq w2 \geqq w3 \geqq \ldots \geqq wn$.

8. The bus system according to claim 2, 3, 4 or 5, wherein:

the first semiconductor and the directional couplers

are mounted on a motherboard;

a plurality of the second semiconductors are mounted on a plurality of daughter boards;

the plurality of daughter boards are connected to the motherboard through connectors; and

intervals of the plurality of daughter boards are constant independently from the lengths of the directional couplers.

9. A memory module for use in the bus system of claim 4 or 5, wherein:

a plurality of memories are mounted instead of the plurality of second semiconductors, directional couplers used for signal transmission between the first semiconductor and the memories are disposed within the memory module, and the memories are arranged at regular intervals within the memory module; and

when it is assumed that intervals between two parallel lines that constitute n directional couplers connected to the bus system are w1, w2, w3, … wn in the order nearer to the first semiconductor, the degrees of coupling of the directional couplers are changed by satisfying $w1 \geqq w2 \geqq w3 \geqq \ldots \geqq wn$, and generated signal amounts of the directional couplers are substantially the same.

10. A bus system using the memory module of claim 9,

wherein:

a data signal is transferred through a data signal bus by using directional couplers disposed within a motherboard, and a control signal is transferred through a control signal bus by using directional couplers disposed within a daughter board;

when it is assumed that lengths of directional couplers in each of n memory modules formed on the motherboard are L1, L2, L3, … Ln in the order nearer to the memory controller, $L1 \leqq L2 \leqq L3 \leqq \ldots \leqq Ln$ is satisfied;

when it is assumed that intervals between two parallel lines that constitute n directional couplers connected to the control signal bus within the memory module are w1, w2, w3, … wn in the order nearer to the first semiconductor, the degrees of coupling of the directional couplers are changed by satisfying $w1 \geqq w2 \geqq w3 \geqq \ldots \geqq wn$, and generated signal amounts of the directional couplers are substantially the same in all of the memories.

11. The bus system according to claim 8, wherein:

the first semiconductor and the directional couplers are mounted on a motherboard;

the plurality of second semiconductors are mounted on a plurality of daughter boards;

the plurality of daughter boards are connected to

the directional couplers of the motherboard through connectors;

a wiring extending from the second semiconductors is folded within the mother board;

when it is assumed that lengths of n directional couplers connected to the bus system are L1, L2, L3, … Ln in the order nearer to the first semiconductor along the wiring, generated signal amounts of the directional couplers are substantially the same by satisfying $L1 \leqq L2 \leqq L3 \leqq \ldots \leqq Ln$.

12. The bus system according to claim 8, wherein:

one bus master is mounted on a motherboard, a plurality of daughter boards are bus-connected to the motherboard through directional couplers and connectors which are disposed within the daughter boards;

the wiring extending from the second semiconductor is folded within the daughter boards;

when it is assumed that lengths of two directional couplers formed in association with parts of the folded main line are L1 and L2 in the order near to the first semiconductor along the wire, a first memory module satisfies $L1 \leqq L2$;

when it is assumed that lengths of two directional couplers formed by the folded wiring and the sub coupling wirings are L3 and L4 in the order nearer to the first

semiconductor along the wiring, a second memory module satisfies L2 ≦ L3 ≦ L4; and

two first memory modules and two second memory modules are mounted on the mother board in the order nearer to the first semiconductor.

13. The bus system according to claim 2 or 4, wherein:

when it is assumed that lengths of n directional couplers connected to the bus system are L1, L2, L3, … Ln in the order nearer to the first semiconductor, L1 ≦ L2 ≦ L3 ≦ … ≦ Ln is satisfied; and

when it is assumed that intervals between two parallel lines that constitute n directional couplers connected to the bus system are w1, w2, w3, … wn in the order nearer to the first semiconductor, the degrees of coupling of the directional couplers are changed by satisfying w1 ≧ w2 ≧ w3 ≧… ≧ wn, and generated signal amounts of the directional couplers are substantially the same.

14. A bus system that transfers data between a plurality of semiconductor devices, wherein:

a first wiring is drawn out of a first semiconductor, a plurality of wirings are arranged in parallel with the first wiring to constitute directional couplers, and the wirings are each connected to a second semiconductor

device;

each of the directional couplers has a different coupling length so that signal amplitudes generated by the plurality of directional couplers may be substantially the same; and

a drive pulse corresponding to a transmitted data signal is inputted to the directional couplers, a signal having a reverse polarity to the data signal is again inputted to the directional couplers with an amplitude that is 10 to 20% of the amplitude of the drive pulse after a reciprocating delay time of the directional couplers, and the signal having the reverse polarity continues until subsequent data is received.

15. A semiconductor device in the bus system of claim 14, wherein:

a high signal or a low signal is outputted to a driver mounted on the first semiconductor or the second semiconductor according to output data;

the semiconductor device includes a delay time holding circuit for holding a reciprocating delay time of the directional couplers used in the bus system; and

the semiconductor device includes a driver that outputs a signal reversing the output data by 10 to 20% of the signal amplitude with the delay time of the holding circuit immediately after the output data is transmitted,

and continuously outputs the signal of the reverse polarity until receiving subsequent data.

16. A main controller in the bus system using the semiconductor of claim 15, comprising:

a plurality of delay time holding circuit which holds a reciprocating wiring length time of the directional couplers connected to the respective memories according to the respective directional couplers; and

a driver which outputs a signal reversing the output data by 10 to 20% of the signal amplitude with the delay time of the holding circuit to the memories immediately after the output data is transmitted to the memories, and continuously outputs the signal of the reverse polarity until receiving subsequent data.

17. A memory in the bus system of claim 15, comprising:

a plurality of delay time holding circuit which holds a reciprocating wiring length time of the directional couplers connected; and

a driver which outputs a signal reversing the output data by 10 to 20% of the signal amplitude with the delay time of the holding circuit immediately after the output data is transmitted, and continuously outputs the signal of the reverse polarity until receiving subsequent data.

18. A memory module in the bus system of claim 15,

wherein memories each having a delay time holding circuit are mounted, each of the memories reads a value of the delay time holding circuit from an EPROM disposed within the memory module prior to data transfer, and all of the memories within the memory module have a value corresponding to the same delay time in the delay time holding circuit.